Amendments to the Claims

1. – 18. (Cancelled)

19. (Currently Amended) An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, including [[an]] a first inverter and a MOS transistor, disposed between the first power supply and the second power supply, for receiving the first input signal; and

a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal while isolating the other one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply.

20. (Previously Presented) The input buffer circuit according to claim 19, wherein the control circuit enables the differential amplifier circuit and disables the second circuit when the first and second input signals have amplitudes smaller than a predetermined voltage.

21. (Previously Presented) The input buffer circuit according to claim 19, wherein the control circuit disables the differential amplifier circuit and enables the second circuit when the first and second input signals have amplitudes greater than a predetermined voltage.

22. (Previously Presented) An input buffer circuit comprising:

a differential amplifier circuit for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, connected to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, including an inverter and a MOS transistor, for receiving the first input signal; and

a control circuit for selectively enabling the differential amplifier circuit and the second circuit in accordance with a control signal, wherein the control circuit enables the differential amplifier circuit and disables the second circuit when the first and second input signals have amplitudes smaller than a predetermined voltage.

23. (Previously Presented) The input buffer circuit according to claim 22, wherein the control circuit disables the differential amplifier circuit and enables the second circuit when the first and second input signals have amplitudes greater than the predetermined voltage.

24. (Previously Presented) The input buffer circuit according to claim 22, wherein the differential amplifier circuit includes a constant current source, and wherein the control circuit disables the differential amplifier circuit by stopping a current from flowing through the constant current source.

25. (Previously Presented) An input buffer circuit comprising:

a differential amplifier circuit for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, connected to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, including an inverter and a MOS transistor, for receiving the first input signal; and

a control circuit for selectively enabling the differential amplifier circuit and the second circuit in accordance with a control signal, wherein the control circuit disables the differential amplifier circuit and enables the second circuit when the first and second input signals have amplitudes greater than a predetermined voltage.

26. (Previously Presented) The input buffer circuit according to claim 25, wherein the control circuit enables the differential amplifier circuit and disables the second circuit when the first and second input signals have amplitudes smaller than the predetermined voltage.

27. (Previously Presented) The input buffer circuit according to claim 25, wherein the differential amplifier circuit includes a constant current source, and wherein the control circuit disables the differential amplifier circuit by stopping a current from flowing through the constant current source.

28. (Currently Amended) An input buffer circuit comprising:

a differential amplifier circuit for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, connected to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, including [[an]] a first inverter and a plurality of MOS ~~transistor~~ transistors, for receiving the first input signal; and

a control circuit for selectively enabling the differential amplifier circuit and the first and second circuits in accordance with a control signal, wherein the differential amplifier circuit and the first circuit are enabled and the second circuit is disabled when the first and second input signals have amplitudes smaller than a predetermined voltage.

29. (Previously Presented) The input buffer circuit according to claim 28, wherein the control circuit disables the differential amplifier circuit and the first circuit

and enables the second circuit when the first and second input signals have amplitudes greater than the predetermined voltage.

30. (Previously Presented) The input buffer circuit according to claim 28, further comprising a driver circuit, connected to the first and second circuits, for receiving an output signal from the enabled one of the first and second circuits enabled by the control circuit.

31. (Currently Amended) The input buffer circuit according to claim 28, wherein ~~each of~~ the first ~~and second circuits~~ circuit includes:

[[an]] a second inverter;

a first PMOS transistor connected between the second inverter and a high-potential power supply; and

[[an]] a first NMOS transistor connected between the second inverter and a low-potential power supply, and

wherein the plurality of MOS transistors include:

a second PMOS transistor connected between the first inverter and a high-potential power supply; and

a second NMOS transistor connected between the first inverter and a low-potential power supply.

32. (Currently Amended) The input buffer circuit according to claim 31, wherein the control circuit generates first and second control signals which are complementary to each other, and wherein the first PMOS transistor of the first circuit and the second NMOS transistor of the second circuit are controlled by the first control signal, and the first NMOS transistor of the first circuit and the second PMOS transistor of the second circuit are controlled by the second control signal.

33. (Currently Amended) An input buffer circuit comprising:

a differential amplifier circuit for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, connected to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, including [[an]] a first inverter and a plurality of MOS ~~transistor~~ transistors, for receiving the first input signal; and

a control circuit, connected to the differential amplifier circuit and the first and second circuits, for selectively enabling the differential amplifier circuit and the first and second circuits in accordance with a control signal, wherein the differential amplifier circuit and the first circuit are disabled and the second circuit is enabled when the first and second input signals have amplitudes greater than a predetermined voltage.

34. (Previously Presented) The input buffer circuit according to claim 33, wherein the control circuit enables the differential amplifier circuit and the first circuit and disables the second circuit when the first and second input signals have amplitudes smaller than the predetermined voltage.

35. (Previously Presented) The input buffer circuit according to claim 33, further comprising a driver circuit, connected to the first and second circuits, for receiving an output signal from the enabled one of the first and second circuits enabled by the control circuit.

36. (Currently Amended) The input buffer circuit according to claim 33, wherein ~~each of~~ the first ~~and second circuits~~ circuit includes:

[[an]] a second inverter;

a first PMOS transistor connected between the second inverter and a high-potential power supply; and

[[an]] a first NMOS transistor connected between the second inverter and a low-potential power supply, and

wherein the plurality of MOS transistors include:

a second PMOS transistor connected between the first inverter and a high-potential power supply; and

a second NMOS transistor connected between the first inverter and a low-potential power supply.

37. (Currently Amended) The input buffer circuit according to claim 36, wherein the control circuit generates first and second control signals which are complementary to each other, and wherein the first PMOS transistor of the first circuit and the second NMOS transistor of the second circuit are controlled by the first control signal, and the first NMOS transistor of the first circuit and the second PMOS transistor of the second circuit are controlled by the second control signal.

38. (Previously Presented) An input buffer circuit comprising:

a differential amplifier circuit for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, disposed between a first power supply and a second power supply, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, including an inverter and a MOS transistor and disposed between the first power supply and the second power supply, for receiving the first input signal; and

a control circuit, coupled to the differential amplifier circuit and the first and second circuits, for selectively enabling the differential amplifier circuit and one of the first circuit and the second circuit in accordance with a control signal while isolating the other one of the first circuit and the second circuit from the first power supply or the second power supply.

39. (Previously Presented) The input buffer circuit according to claim 38, wherein the control circuit isolates the first circuit from the first power supply or the second power supply when the first and second input signals have amplitudes smaller than a predetermined voltage.

40. (Previously Presented) The input buffer circuit according to claim 38, wherein the control circuit isolates the second circuit from the first power supply or the second power supply when the first and second input signals have amplitudes greater than a predetermined voltage.

41. (Previously Presented) The input buffer circuit according to claim 38, wherein the control circuit enables the differential amplifier circuit and the first circuit and disables the second circuit when the first and second input signals have amplitudes smaller than a predetermined voltage.

42. (Previously Presented) The input buffer circuit according to claim 38, wherein the control circuit disables the differential amplifier circuit and the first circuit and enables the second circuit when the first and second input signals have amplitudes greater than a predetermined voltage.

43. (Previously Presented) An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, including an inverter and a MOS transistor and disposed between the first power supply and the second power supply, for receiving the first input signal and generating an output signal to the first circuit; and

a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal and disabling the other one of the differential amplifier circuit and the second circuit in accordance with the control signal.

44. (Previously Presented) An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, including an inverter and a MOS transistor and disposed between the first power supply and the second power supply, for receiving the first input signal and generating an output signal to the first circuit; and

a control circuit for selectively isolating one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply while enabling the other one of the differential amplifier circuit and the second circuit.

45. (Previously Presented) An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, including an inverter and a MOS transistor and disposed between the first power supply and the second power supply, for receiving the first input signal and generating an output signal to the first circuit; and

a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal while isolating the other one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply.

46. (Previously Presented) An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating a single amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, including an inverter and a MOS transistor and disposed between the first power supply and the second power supply, for receiving the first input signal and generating a single output signal to the first circuit; and

a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal and disabling the other one of the differential amplifier circuit and the second circuit in accordance with the control signal.

47. (Previously Presented) An input buffer circuit comprising:

a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating a single amplified signal corresponding to a voltage difference between the first and second input signals;

a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit;

a second circuit, including an inverter and a MOS transistor and disposed between the first power supply and the second power supply, for receiving the first input signal and generating a single output signal to the first circuit; and

a control circuit for selectively isolating one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply while enabling the other one of the differential amplifier circuit and the second circuit.

48. (Previously Presented) The input buffer circuit according to claim 19, wherein each of the first and second circuits includes only one output terminal.

49. (Previously Presented) The input buffer circuit according to claim 28, wherein each of the first and second circuits includes only one output terminal.

50. (Currently Amended) The input buffer circuit according to claim 28, wherein the first circuit includes:

[[an]] a second inverter; and

a PMOS transistor connected between the second inverter and a high-potential power supply.

51. (Currently Amended) The input buffer circuit according to claim 28, wherein the first circuit includes:

[[an]] a second inverter; and

an NMOS transistor connected between the second inverter and a low-potential power supply.

52. (Currently Amended) The input buffer circuit according to claim 28, wherein ~~the second circuit includes:~~

~~an inverter; and~~

one of the plurality of MOS transistors is a PMOS transistor connected between the first inverter and a high-potential power supply.

53. (Currently Amended) The input buffer circuit according to claim 28, wherein ~~the second circuit includes:~~

~~an inverter; and~~

one of the plurality of MOS transistors is an NMOS transistor connected between the first inverter and a low-potential power supply.

54. (Currently Amended) The input buffer circuit according to claim 19, wherein the first circuit includes [[an]] a second inverter.

55. (Currently Amended) The input buffer circuit according to claim 19, wherein the MOS transistor is a PMOS transistor and is connected between the first inverter and the first power supply.

56. (Currently Amended) The input buffer circuit according to claim 19, wherein the MOS transistor is an NMOS transistor and is connected between the first inverter and the second power supply.

57. (Currently Amended) The input buffer circuit according to claim 19, wherein the first circuit receives an output signal from the enabled one of the differential amplifier circuit and the second circuit.

58. (Previously Presented) The input buffer circuit according to claim 38, wherein the MOS transistor is a PMOS transistor and is connected between the inverter and the first power supply.

59. (Previously Presented) The input buffer circuit according to claim 38, wherein the MOS transistor is an NMOS transistor and is connected between the inverter and the second power supply.